AMENDMENTS TO THE CLAIMS

Please cancel Claims 1, 8, 12 and 18.

Please amend Claims 3, 7, 9, 11, 16, 19, 20, 23, 28-30, 55, 60 and 63 and add new Claim 67 as indicated below.

1. (Canceled)

2. (Canceled)

3. (Currently Amended) The method of Claim [[1]] 9, wherein forming no more than about one monolayer comprises supplying a first chemistry substantially excluding the second reactant species [[and]], reacting comprises supplying a second chemistry substantially excluding the first reactant species and exposing comprises supplying a third chemistry substantially excluding the second reactant species.

4. (Currently Amended) The method of Claim 3, further comprising repeatedly alternating supplying the first chemistry, [[and]] supplying the second chemistry and supplying the third chemistry until a dielectric layer forms having a thickness between about 10 Å and 200 Å.

5. (Currently Amended) The method of Claim 3, further comprising supplying a carrier gas while repeatedly alternating supplying the first chemistry, [[and]] supplying the second chemistry and supplying the third chemistry.

6. (Currently Amended) The method of Claim 5, wherein the carrier gas purges reactants between supplying the first chemistry and supplying the second chemistry and between supplying the second chemistry and supplying the third chemistry.

7. (Original) The method of Claim 6, wherein supplying the first chemistry is stopped and the reaction chamber is purged with more than about two chamber volumes of purge gas before supplying the second chemistry.

8. (Canceled)

9. (Currently Amended) [[The method of Claim 8,]] A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and

depositing a high k dielectric layer directly over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species;

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material; and

exposing the second material to a third reactant species to leave no more than about one monolayer of a third material, wherein the dielectric layer comprises two different metals and oxygen.

10. (Original) The method of Claim 9, wherein the dielectric layer comprises a metal, silicon and oxygen.

11. (Currently Amended) The method of Claim [[1]] 9, wherein the dielectric layer has a dielectric constant of greater than about 10.

12. (Canceled)

13. (Original) The method of Claim 11, wherein the dielectric layer has a dielectric constant equal to or greater than about 20.

14. (Currently Amended) The method of Claim [[1]] 9, wherein the first material is self-terminated.

15. (Original) The method of Claim 14, wherein the first material is terminated by halide ligands.

16. (Currently Amended) [[The method of Claim 15,]] A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and

depositing a high k dielectric layer directly over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species, the first material being self-terminated with halide ligands; and

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material, wherein the first reactant species comprises a zirconium halide and the second reactant species comprises an oxygen-containing source gas.

17. (Original) The method of Claim 14, wherein the first material is terminated by organic ligands.

18. (Canceled)

19. (Currently Amended) [[The method of Claim 1,]] A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and

depositing a high k dielectric layer directly over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species, the first material being self-terminated with halide ligands; and

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material, wherein the first material comprises ethoxide-terminated tantalum and the second reactant species comprises an oxygen-containing source gas.

20. (Currently Amended) The method of Claim [[1]] 9, further comprising forming a barrier layer directly on the textured silicon surface prior to forming no more than about one monolayer.

21. (Original) The method of Claim 20, wherein forming a barrier layer comprises nitriding the textured silicon surface.

22. (Original) The method of Claim 20, wherein forming a barrier layer comprises oxidizing the textured silicon surface to form a silicon oxide and nitriding the silicon oxide.

23. (Currently Amended) The method of Claim [[1]] 9, wherein bottom electrode conforms to a three-dimensional folding structure.

24. (Original) The method of Claim 23, wherein the bottom electrode conforms to a trench within a semiconductor substrate.

25. (Original) The method of Claim 23, wherein the three-dimensional folding shape is formed above a semiconductor substrate.

26. (Original) The method of Claim 25, wherein the three-dimensional shape defines an interior volume.

27. (Original) The method of Claim 26, wherein the three-dimensional shape conforms to a cylinder.

28. (Currently Amended) The method of Claim [[1]] 9, further comprising depositing a conductive layer over the dielectric layer, wherein depositing the conductive layer comprises:

forming no more than about one monolayer of a [[third]] fourth material over the dielectric layer by exposure to a [[third]] fourth reactant species; and

reacting a [[fourth]] fifth reactant species with the [[third]] fourth material to leave no more than about one monolayer of a [[fourth]] fifth material.

29. (Currently Amended) The method of Claim 28, wherein the [[third]] fourth reactant species comprises a metal complex, the [[fourth]] fifth reactant species comprises a nitrogen-containing source gas, and the conductive layer comprises a metal nitride.

30. (Currently Amended) A method of forming a dielectric layer having a dielectric constant greater than or equal to about [[10]] 20 directly over a textured silicon bottom electrode having a hemispherical grain (HSG) morphology in an integrated circuit, comprising:

forming no more than about one monolayer of a metal-containing species in a self-limited reaction; and

reacting an oxygen-containing species with the monolayer.

31. - 32. (Cancelled)

33. (Original) The method of Claim 30, wherein the self-limited reaction comprises forming a halogen-terminated metal film.

34. (Original) The method of Claim 33, wherein reacting the oxygen-containing species comprises a ligand-exchange reaction.

35. (Original) The method of Claim 30, further comprising repeating forming no more than about one monolayer and reacting the oxygen-containing species at least about 10 times until the dielectric layer has a desired thickness.

36. - 54. (Canceled)

55. (Currently Amended) A process of forming a capacitor dielectric having a dielectric constant of greater than or equal to about [[10]] 20 over a hemispherical grain silicon surface, comprising:

directly coating the hemispherical grain silicon surface with no more than about one monolayer of a ligand-terminated metal complex in a first phase;

replacing ligands of the ligand-terminated metal with oxygen in a second phase distinct from the first phase; and

repeating the first and second phases in at least about 10 cycles.

56. (Original) The process of Claim 55, wherein each cycle comprises a third phase, the third phase comprising adsorbing no more than about one monolayer of a second ligand-terminated metal after the second phase.

57. (Original) The process of Claim 56, wherein each cycle further comprises a fourth phase, the fourth phase comprising replacing ligands of the second ligand-terminated metal with oxygen.

58. (Original) The process of Claim 57, wherein the first phase comprises pulsing a first oxygen-containing species.

59. (Original) The process of Claim 58, wherein the fourth phase comprises pulsing a different oxygen-containing species.

60. (Currently Amended) [[The process of Claim 55]] A process of forming a capacitor dielectric having a dielectric constant of about 10 over a hemispherical grain silicon surface, comprising:

directly coating the hemispherical grain silicon surface with no more than about one monolayer of a ligand-terminated metal complex in a first phase;

replacing ligands of the ligand-terminated metal with oxygen in a second phase distinct from the first phase; and

repeating the first and second phases in at least about 10 cycles, wherein the ligand-terminated metal comprises a metal ethoxide complex.

61. (Original) The process of Claim 55, wherein the ligand-terminated metal comprises a metal chloride complex.

62. (Original) The process of Claim 55, comprising maintaining a temperature of less than about 350°C.

63. (Currently Amended) A method of forming a capacitor with high surface area in an integrated circuit, comprising:

forming a bottom electrode in a three-dimensional folding shape;

superimposing a hemispherical grain silicon layer over the three-dimensional folding shape; and

depositing a high k dielectric layer conformally directly over the textured morphology by cyclically supplying at least [[two]] three alternating, self-terminating chemistries, wherein no more than one monolayer is formed per cycle, and wherein the dielectric layer comprises silicon, oxygen and a metal.

64. - 66. (Canceled)

67. (New) A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and

depositing a high k dielectric layer directly over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species; and

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material, and

wherein the dielectric layer is selected from the group consisting of tantalum oxide, titanium oxide, zirconium oxide, niobium oxide, hafnium oxide and mixtures and compounds thereof.